

IN THE CLAIMS

1. (Currently Amended) A cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, said cache memory comprising:

a modifier that modifies modification unit operable to modify the order data regardless of an actual access order; and

a selector that selects selection unit operable to select, based on the modified order data, a cache entry to be replaced,

wherein said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present, and

wherein said selector selects the cache entry to be replaced in accordance with the order data when the cache entry having the oldest-order flag attached is not present.

2. (Currently Amended) The cache memory according to claim Claim-1,

wherein said modifier comprises modification unit includes:

a specifier that specifies specifying unit operable to specify a cache entry that holds data which is within an address range specified by a processor; and

an oldest-orderer that causes oldest-ordering unit operable to cause the order data of the specified cache entry to be become oldest in the access order, regardless of the actual access order.

3. (Currently Amended) The cache memory according to claim Claim-2, wherein said specifier comprises specifying unit has:

a first converter that converts conversion unit operable to convert a starting address of the

address range to a start line address that indicates a starting line within the address range when;

in the case where the starting address indicates a midpoint in line data;

a second converter that converts conversion unit ~~operable to convert~~ an ending address of the address range to an end line address that indicates an ending line within the address range when; in the case where the ending address indicates the a midpoint in the line data; and

a judger that determines judgment unit ~~operable to judge~~ whether or not there is a cache entry that holds data corresponding to each line address from the start line address to the end line address.

4. (Currently Amended) The cache memory according to claim ~~Claim~~ 3,

wherein said oldest-orderer attaches oldest-ordering unit ~~is operable to attach~~, to the order data, the ~~an~~ oldest-order flag which indicates that the access order is oldest.

5. (Cancelled).

6. (Currently Amended) The cache memory according to claim ~~4~~ ~~Claim~~ 5,

wherein the cache entry has, as the order data, a 1-bit order flag that indicates whether the access order is old or new, and

wherein said selector selects selection unit ~~is operable to select~~ as the cache entry ~~[[.]]~~ to be replaced, the cache entry in which the order flag indicates old when the, in the case where a cache entry having that has the oldest-order flag attached is not present.

7. (Currently Amended) The cache memory according to claim ~~Claim~~ 1,

wherein said modifier modifies modification unit ~~is operable to modify~~ the order data so

that one cache entry is indicated as an shows Nth cache entry in the access order, wherein and

N is a number indicating any one of: (a) a number indicating an the oldest cache entry in the access order; (b) a number indicating a the newest cache entry in the access order; (c) a number indicating an Nth cache entry from the oldest in the access order; and (d) a number indicating an Nth cache entry from the newest cache entry in the access order.

8. (Currently Amended) The cache memory according to claim Claim-1, wherein said modifier modification unit comprises has:

an instruction detector that detects detection unit operable to detect that a memory access instruction that includes a modification directive for the access order has been executed; and
a rewriter that rewrites rewrite unit operable to rewrite the order data for a cache entry that is accessed due to the memory access instruction.

9. (Currently Amended) The cache memory according to claim Claim-1, wherein said modifier comprises modification unit includes:

a holder that holds holding unit operable to hold an address range specified by a processor;
a searcher that searches searching unit operable to search for a cache entry that holds data corresponding to the address range held in said holding unit; and
a rewriter that rewrites rewrite unit operable to rewrite the order data so that the access order of the cache entry searched for by said searcher searching unit is an Nth cache entry in the access order.

10. (Currently Amended) A control method for controlling a cache memory which holds, in each

cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, said method comprising:

~~a modification step for modifying the order data regardless of an actual access order; and~~
~~a selecting step for selecting, based on the modified order data, a cache entry to be replaced,~~

wherein the cache entry to be replaced is selected when a cache miss occurs and a cache entry having an oldest-order flag attached is present, and

wherein the cache entry to be replaced is selected in accordance with the order data when the cache entry having the oldest-order flag attached is not present.